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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/683,631	10/10/2003	Inkuk Kang	H0712	1197

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EXAMINER	
ECKERT II, GEORGE C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/683,631	KANG ET AL.	
	Examiner	Art Unit	
	George C. Eckert II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-19,21-37,39 and 40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-19,21-37,39 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed January 13, 2005 in which claims 1 and 18 were amended and claims 3, 20 and 38 canceled has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4, 7, 12, 13, 15, 17, 18, 21, 25, 29-31, 34 and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by 4,243,997 to Natori et al. Natori teaches in figure 3 a device comprising:

a semiconductor substrate 11 having at least one trench formed therein (trench formation in figure 2d);

a recessed channel region 31 of a first conductivity type semiconductor (p-type) formed in the substrate below the trench;

a source and a drain region 15 and 16 both of second conductivity (n-type) formed in the substrate on opposing sides of the trench, wherein a bottom of the source and drain regions are above the floor of the trench (as seen in figure 3 and col. 2, lines 41-43);

a gate dielectric layer 17 formed on the substrate, the gate dielectric layer formed along the bottom and sidewalls of the trench; and

a control gate 18 formed over the dielectric layer above the recessed region,

wherein the bottom of the source and drain regions are at a depth from the surface of about 40 to 60 percent of the depth of the floor of the trench from the surface (Natori teaches the trench is formed to the depth of the intrinsic layer 11 which depth is 1.2μm (col. 2, lines 58-61, col. 3, lines 12-15) and that the source/drain region are formed to a depth of 0.5μm (col. 3, lines 20-23) so that the ratio is 0.5/1.2 = 41.6%).

Regarding claims 4 and 21, Natori teaches in figure 2c that the trench is formed using a thermal oxidation 26 and show in figure 3 that the trench has a rounded bottom at the corners such that the angle at the corner is greater than 90° with respect to the floor. Regarding claims 7 and 25, the substrate 11 used by Natori is a bulk silicon substrate. Regarding claims 12 and 29, Natori teaches in figure 3 that the gate dielectric layer 17 extends above the source and drain regions. Regarding claims 13 and 30, Natori teaches in figure 3 that the gate resides in the trench. Regarding claims 15 and 31, Natori teaches that the gate dielectric 17 is comprised of SiO_2 (col. 2, lines 44-45), which is a standard-k dielectric material. Regarding claims 17 and 34, Natori teaches in figure 3 that the upper surface of the gate is "substantially" at the same level as the upper surface of the gate dielectric. Regarding claims 39 and 40, Natori teaches in figure 3 that the trench is "substantially" rectangular.

3. Claims 1, 2, 4, 7, 13, 15, 18, 19, 21, 25, 30 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by 6,528,847 to Liu. Liu teaches in figures 1A-M the formation of a device comprising:

a semiconductor substrate 12 having at least one trench 24 formed therein (trench formation in figure 1d);

a recessed channel region 24 of a first conductivity type semiconductor (p-type) formed in the substrate below the trench (fig. 1C);

a source and a drain region 64 both of second conductivity (n-type) formed in the substrate on opposing sides of the trench, wherein a bottom of the source and drain regions are above the floor of the trench (as seen in figure 1K);

a gate dielectric layer 34 formed on the substrate, the gate dielectric layer formed along the bottom and sidewalls of the trench; and

a control gate 36 formed over the dielectric layer above the recessed region,

wherein the bottom of the source and drain regions are at a depth from the surface of about 40 to 60 percent of the depth of the floor of the trench from the surface (Liu teaches the trench is formed to a depth d_c of between .05 - .25 μm (col. 6, line 63) and that the source/drain regions are formed to a depth d_j of less than 0.1μm (col. 8, lines 65-66) so that the ratio may be for example .09/.225 = 40% to .09/.15 = 60%).

Regarding claims 2 and 19, Liu teaches that d_j may be less than .1 μm and d_c is between .05 and .25 μm such that a difference is between .07 and .1 μm. Regarding claims 4 and 21, Liu teaches in figure 1c that the trench is formed using a thermal oxidation 22 and has sloped sides such that the angle of the sidewalls is greater than 90° with respect to the floor. Regarding

claims 7 and 25, the substrate 12 used by Liu is a bulk silicon substrate. Regarding claims 13 and 30, Liu teaches in figure 1M that the gate resides in the trench. Regarding claims 15 and 31, Liu teaches that the gate dielectric 34 is comprised of SiO_2 (col. 7, lines 34), which is a standard-k dielectric material.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4, 7-10, 12, 13, 17-19, 21, 25-27, 29, 30, 34, 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,661,053 to Willer et al. (hereinafter "Willer"). Willer teaches in figures 2-4 a memory device and method of forming the device comprising:

a semiconductor substrate 1 having at least one trench formed in a surface thereof;

a recessed channel region 5 of a first conductivity type semiconductor (p-type) formed in the substrate below each trench;

a source region 2 and a drain region 3 of a second conductivity type (n-type) formed in the semiconductor substrate on opposing sides of each trench, wherein a bottom of the source and drain regions are above a floor of the trench;

a gate dielectric layer 10-12 formed on the substrate along the bottom and sidewalls of the trench; and

a control gate 4 formed over the dielectric layer above the recessed channel region.

Regarding claims 1, 2, 18 and 19, Willer teaches in column 5, lines 47-52 the depths of the source/drain regions and that of the trench, wherein the source/drain depth may be 150 nm (1500Å) and the trench depth may be 220 nm (2200 Å) so that a difference is 700Å and a proportion is 150/220 or 68%. While 68% is not absolutely within the range of 40-60% as instantly claimed, the slight difference in changing the depth of either the gate trench or the source/drain regions is considered obvious as a mere optimization of that already known. Furthermore, since there is no showing of a new and unexpected result achieved by the claimed depth ratio, the claims are not considered patentable over Willer. See *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (citing *In re Aller*, since underlying structure is known in the art, patentability must lie in the specific dimensions of the instant claims; however, if dimension modification was within the capability of one skilled in the art, the new dimensions must produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art.).

Regarding claim 4, Willer teaches in figure 4 an embodiment in which the trench sidewall has an angle greater than 90° to the trench floor. Regarding claim 7, Willer teaches the device formed in a bulk substrate. Regarding claims 8-10, Willer teaches that the dielectric layer is ONO such that the nitride layer is isolated from the bottom and side of the trench and that the gate and substrate are silicon as to form a SONOS device. Regarding claim 12, Willer teaches the gate dielectric is formed to extend above the source and drain (e.g. fig. 4). Regarding claim 13, Willer teaches the control gate resides within the trench and is substantially at the same level as an upper surface of the gate dielectric (note that layer 13 is the word line while 4 is the gate).

Regarding claims 39 and 40, Willer teaches in column that the trench is substantially rectangular (e.g. a rectangle with a rounded bottom).

5. Claims 5, 6, 11, 14-16, 22-24, 28, 31-33, 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over '053 to Willer as applied above in view of 2002/0024092 to Palm et al. (hereinafter "Palm"). Willer taught the device and method of claims 1 and 18 but did not teach the specific thickness or alternative types of the dielectric layer, nor the specific process for etching the trench. Palm teaches a device comprising and a method of forming a memory cell wherein the bottom of the source/drain regions are above the bottom of a gate filled trench, which trench is located in a substrate. Palm further teaches a list of dielectrics in paragraphs 0014-16 which include both high-K and standard-K materials. Palm teaches that a total thickness of the dielectric may be between 65 – 250Å and comprise an ONO layer wherein the bottom oxide layer has a thickness from 25 – 80 Å (para. 0029). Palm also teaches that the trench may be formed by an anisotropic (directional) etch (fig. 7, para. 0034) and an RIE etch is considered well known and obvious in the art. Also, forming the device on an SOI substrate as opposed to bulk is considered well known in the art as an SOI substrate provides better isolation between devices.

Willer and Palm are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the dielectrics taught by Palm in the device of Willer. The motivation for doing so, as is taught by Palm, is that the list of dielectrics allows for optimization of both the electron storing ability of the layer and the dielectric constant of the layer (para. 0013). Therefore, it would have been

obvious to combine Willer and Palm to obtain the invention of claims 5, 6, 11, 14-16, 23, 24, 26-28 and 31-33.

6. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over '053 to Willer in view of 5,960,271 to Wollesen et al. (hereinafter "Wollesen"). Willer taught the method of claims 18 and 34 but did not expressly disclose that the gate was made substantially at the same level as the upper surface of the gate dielectric layer by CMP. Wollesen teaches in figures 7b-9 a gate dielectric 20a and gate layer 21 which are formed in a trench in a substrate, wherein the dielectric and gate are planarized using a CMP process (fig. 9, col. 5, lines 31-43).
Willer and Wollesen are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to perform the method of Willer further including the CMP process of Wollesen. The motivation for doing so, as is taught by Wollesen, is that a CMP process is well known in the art and allows for use of the overlying oxide layer as an etch stop (col. 5, lines 31-37). Therefore, it would have been obvious to combine Willer and Wollesen to obtain the invention of claim 35.

Response to Arguments

7. Applicant's arguments with respect to claims 1 and 18 have been considered but are moot in view of the new ground(s) of rejection. As stated in the above rejection over Willer, now made under section 103, applicant's claimed ratio of the source/drain depth to the gate trench depth, while not anticipated, is considered obvious over Willer as merely a change in dimension without a showing of unexpected results. Applicant has pointed out that the difference in depth

does increase channel length which reduces short channel effects. However, because the channel length of Willer must be greater than that instantly claimed (based on the ratio being above 60%), such advantages were already known in the art. If anything, applicant has shortened the channel length over that known in the art but has not provided any unexpected results for that change.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (571) 272-1728.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GEORGE ECKERT
PRIMARY EXAMINER